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Amendment C

REMARKS

Responsive to the Office Action mailed December 8, 2005, Applicant provides the above amendments and following remarks. The claims have been amended without adding new matter. Claims 6 and 14-18 have been amended to correct minor typographical errors, and claim 2 and 4 were previously cancelled. Therefore, sixteen (16) claims remain pending in the application: claims 1, 3, and 5-18. Reconsideration of claims 1, 3, and 5-18 in view of the amendments above and remarks below is respectfully requested.

By way of this amendment, Applicant has made a diligent effort to place the claims in condition for allowance. However, should there remain any outstanding issues that require adverse action, it is respectfully requested that the Examiner telephone the undersigned at (858) 552-1311 so that such issues may be resolved as expeditiously as possible.

Claim Objections

1. Claim 6 stands objected to because line 14 recites "implement" instead of "implements". Applicant has amended claim 6 to replace "implement" with --implements--.

Claim Rejections - 35 U.S.C. §112

2. Claims 14-18 stand rejected under 35 U.S.C. § 112, second paragraph, as failing to particularly point out and distinctly claim that which Applicant regard as the invention. Applicant has amended claims 14-18 such that the preamble references back to the "system" of claim 13 instead of an apparatus. Therefore, proper antecedent basis is provided.

Claim Rejections - 35 U.S.C. §102

3. Claims 6-18 stand rejected under 35 U.S.C. § 102(b), as being anticipated by U.S. Patent No. 4,968,977 (Chinnaswamy et al.). Applicant respectfully submits, however, that the Chinnaswamy patent does not teach each element of at least independent claims 6 and 13.

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More specifically, claim 6 recites in part, for example, "a first hybrid switching module comprising ... a first switch ... and a first bridge ... wherein the first switch selectively couples to the first bridge and selectively couples to the input/output link data channel" The Examiner in rejecting claim 6 equates "Fig. 2, item 32" of the Chinnaswamy patent to both the claimed first hybrid switching module as well as to the claimed first switch. The Examiner then suggests that "item 6" of the Chinnaswamy patent is equivalent to the "first bridge" of claim 6. However, "item 32" is not equivalent to a first switch as claimed, nor does "item 32" include a first switch as claimed. The Chinnaswamy patent does not teach a first hybrid switching module that comprises both a first switch and a first bridge, and thus claim 6 is not anticipated.

Further, Chinnaswamy patent fails to teach or suggest a switch that selectively couples with the first bridge. "Item 32" does not selectively couple with "item 6", and instead "item 6" is part of "item 32". Applicant respectfully submits that the Chinnaswamy patent does not teach at least a first switch, a first switch that selectively coupled with a first bridge as recited in claim 6, or a first switch that selectively couples with the input/output link data channel. Thus, the Chinnaswamy patent fails to teach each element of claim 6, and claim 6 is not anticipated.

Additionally, the Examiner in rejecting claim 6 equates "item 6" of Fig. 3 of the Chinnaswamy patent to the claimed "first bridge" and additionally equates "item 38 (I/O1)" to the first hybrid switching module main data channel. The Examiner then suggests that the "item 6" is "coupled to the first hybrid switching module main data channel [item 38 (I/O1)]." (Office Action, paragraph 9). However, "item 6" does not couple with "item 38 (I/O1)". Therefore, the Chinnaswamy patent does not teach the first bridge ("item 6" as defined by the Examiner) coupled with the first hybrid switching module main data channel ("item 38 (I/O1)" as defined by the Examiner), and thus claim 6 is not anticipated by the Chinnaswamy patent.

Claim 13 was also rejected based on the same analysis of the Chinnaswamy patent. Therefore, claim 13 is also not anticipated by the Chinnaswamy patent for at least the reasons provided above. Additionally, claim 13 recites in part, for example:

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a failure mode that couples the input/output link data channel with the first hybrid switching module bus data channel during a failure allowing external access to the first peripheral device providing the first function during the failure.

The Chinnaswamy patent does not teach or suggest a failure mode that couples the input/output link data channel with the first hybrid switching module bus data channel during a failure.

Instead, the Chinnaswamy patent only describes generating "a 'wait list' or queue ... containing commands that have not been executed due to the unavailability of source, destination" (Chinnaswamy patent, column 18, lines 45-47). This "wait list" is not a failure mode that couples the input/output link data channel with the first hybrid switching module bus data channel during a failure. To the contrary, the Chinnaswamy patent only generates a backlog of commands when a source or destination is unavailable. The Examiner cites column 4, lines 65 through column 5 line 11 of the Chinnaswamy patent in attempting to demonstrate support for the contention that the Chinnaswamy patent describes a failure mode. However, this portion of the Chinnaswamy patent only states that a "controller monitors the availability of data transaction paths by recognizing when ... nodes become unavailable...." This is not a failure mode but just a recognition of unavailable nodes. As demonstrated above, the Chinnaswamy patent only generates a "wait list" when nodes are unavailable. The Chinnaswamy patent further elaborates on this unavailability at column 18, lines 56-60 where "[i]f it is found that ... nodes are not available ... step 102 is accessed for that command to store that command in a 'wait list'" (Emphasis added). As such, the Chinnaswamy patent does not teach or suggest a "failure mode", and further fails to teach a failure mode that couples the input/output link data channel with the first hybrid switching module bus data channel during a failure as recited in claim 13. Therefore, the Chinnaswamy patent does not teach each element of claim 13, and thus, fails to anticipate claim 13.

4. Claims 6-18 stand rejected under 35 U.S.C. § 102(b), as being anticipated by U.S. Patent No. 4,014,005 (Fox et al.). Applicant respectfully traverses this rejection.

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Regarding claim 6, the Examiner indicates that in the Fox patent a line depicted in FIG. 1 extending between a "Crossbar Switch 1" and a "Crossbar Switch M" of FIG. 1 is equal to the claimed "input/output link data channel". However, this "line" is only inputs to the "Crossbar Switch 1" and "Crossbar Switch M", and is not input/output between the Switches. Further, this "line" is actually connected from a Processor 1 (Channel C) to an input of Crossbar Switch 1, and from Processor 1 to an input of Crossbar Switch M. These are inputs from Processor 1 and are not input/outputs between "Crossbar Switch 1" and "Crossbar Switch M". The Fox patent fails to teach or suggest an I/O connection between "Switch 1" and "Switch M", and thus, the line extending between Crossbar Switch 1 and Crossbar Switch M is not an "input/output link data channel" as recited in claim 6.

Further, the Examiner indicates that a first bridge (a "decoder section" shown in FIGS. 5 and 5A of the Fox patent) couples with a "main data channel". However, the Examiner indicated that the "main data channel" in FIG. 1 was an output "item 2" of the Crossbar Switch 1. The "decoder section" of FIG. 5 does not couple with the outputs of the Crossbar Switch 1 and thus does not couple with what the Examiner previously defined as the "main data channel." Additionally, the "decoder section" only receives control signals to control switches (1-4) within the Crossbar Switch 1 (see FIG. 5), and does not couple with the "main data channel" (as defined by the Examiner). Therefore, the "decoder section" is not a "first bridge" as claimed and does not couple with what the Examiner defines as the "main data channel".

Still further with respect to the Fox patent, the Examiner suggests that the first switch (referring to items within the Crossbar Switch 1 of FIGS. 5 and 5A) selectively couples to the first bridge (defined by the Examiner as the "decoder section") and selectively couples to the input/output link data channel (defined by the Examiner as the connection between the inputs of the Crossbar Switches 1 and M (identified above as only inputs with no communication between Crossbar Switches)). However, the "first switch" does not selectively couple with the "decoder section" because the switches (1-4) of the Crossbar Switch shown in FIG. 5 always couple with the "decoder section" and receive control from the "decoder section". The "decoder section" is not a bridge as recited in claim 6. Further, the "decoder section" does not couple with a main

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data channel as recited in claim 6, but instead the "decoder section" just "receive[s] the control signals from the CACU." (Fox patent, col. 11, lines 21-22). Additionally, the first switch defined by the Examiner does not selectively couple the "processor data channel" with the first bridge ("decoder section") because the "decoder section" only received control signals.

Therefore, the Fox patent fails to teach each element of claim 6, and thus, claim 6 is not anticipated by the Fox patent.

Independent claim 13 includes similar claim language as that of claim 6, and thus claim 13 is also not anticipated by the Fox patent for at least the reasons provided above. Further, the Fox patent does not teach at least a "failure mode that couples the first input/output link data channel with the first main bus when the first processor fails" as recited in claim 13. The Examiner cites column 1, lines 55-58, and column 3, lines 7-13 of the Fox patent in attempting to show a failure mode. However, column 1, lines 55-58 of the Fox patent is not associated with a failure, and Applicant assumes the Examiner intended column 2, lines 55-58, and column 3, lines 7-13. These portions of the Fox patent, however, do not teach or suggest the "failure mode that couples the first input/output link data channel with the first main bus when the first processor fails" as recited in claim 13, but instead only describes duplicate copies of the same configure information that can be used to later restore a processor. This does not teach the failure mode that couples the first input/output link data channel with the first main bus as recited in claim 13. Therefore, the Fox patent fails to teach each element of claim 13, and thus, claim 13 is not anticipated by the Fox patent.

Claim Rejections - 35 U.S.C. §103

5. Claims 1, 3 and 5 stand rejected under 35 U.S.C. § 103(a), as being unpatentable over the Chinnaswamy patent in view of U.S. Patent No. 6,038,630 (Foster et al.), and unpatentable over the Fox patent in view of U.S. Patent No. 6,038,630 (Foster et al.).

Independent Claim 1 includes claim language similar to that of independent claims 6 and 13. Therefore, the Chinnaswamy and Fox patents fail to teach each element of

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claim 1 for at least the reasons provided above. Further, the Foster patent fails to teach those elements demonstrated above as not being taught by the Chinnaswamy and Fox patents. Therefore, neither the combination of the Chinnaswamy and Foster, nor the combination of the Fox and Foster patent teaches each element of independent claim 1.

Section 2143.03 of the MPEP states that in order "to establish a prima facie case of obviousness of a claimed invention, all of the claimed limitations must be taught or suggested by the prior art." Therefore, a prima facie case of obviousness is not met by the combinations of the Chinnaswamy and Foster patents, or the Fox and Foster patents as the combinations do not teach or suggest all of the limitations of claim 1 (MPEP § 2143.03). Thus, Applicant respectfully submits the rejection is overcome and should be withdrawn.

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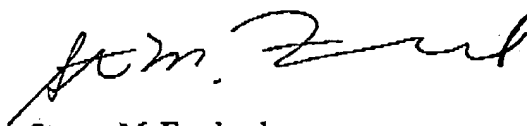
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CONCLUSION

Applicant submits that the above amendments and remarks place the pending claims in a condition for allowance. Therefore, a Notice of Allowance is respectfully requested.

Respectfully submitted,

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